CLAIMS

What is claimed is:

Sub A17

1. A chip scale integrated circuit chip package comprises a die mounted by flip chip interconnection to a first surface of a package substrate, and second level interconnections formed on the first surface of the package substrate.

2. The package of claim 1 wherein the die is provided with interconnection bumps affixed to an arrangement of connection sites in a first surface of the die, and the flip chip interconnection is made by apposing the first surface of the die with the first surface of the package substrate and bringing the interconnect bumps into contact with a complementary arrangement of interconnect pads on the first surface of the substrate under conditions that promote bonding of the bumps on the pads.

3. The package of claim 1 wherein a gap between the first surface of the die and the first surface of the substrate is at least partly filled with a die attach material.

4. The package of claim 1 wherein the height of the second level interconnections defines a standoff, and the sum of a thickness of the first die and a gap between the first surface of the die and the first surface of the substrate is less than the standoff.

5. The package of claim 1 wherein the connection of the interconnect bumps and the pads is a solid state connection, made by applying heat and mechanical force to deform the bumps against the pads without melting either mating surface.

6. The package of claim 1 wherein the first die is attached at about the center of the first surface of the substrate, and the solder balls for the second level interconnections are located nearer the periphery of the substrate.

7. The package of claim 1 wherein a ground plane is optionally provided on the second surface of the substrate.

8. The package of claim 1 wherein at least some electrical traces are constructed as coplanar waveguides.

9. The package of claim 1, further comprising a second die attached to a second surface of the substrate.

10. The package of claim 9 wherein the second die is interconnected to the substrate by wire bonding.

11. The package of claim 9 wherein the second die is interconnected to the substrate by a flip-chip interconnect.